UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,750	03/15/2001	Huy Thanh Vo	303.723US1	4340

21186 7590 01/30/2006

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
1600 TCF TOWER
121 SOUTH EIGHT STREET
MINNEAPOLIS, MN 55402

EXAMINER
MAI, SON LUU

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,750	VO, HUY THANH	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005 and 08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41 and 45-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41 and 45-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments filed 11-30-05 and 12-08-05 have been entered. Accordingly claims 1-41 and 45-57 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8-14, 15-18, 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

4. Regarding claim 1, Cowles discloses a memory array (figure 2A), comprising:

- a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region;
- a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell;
- a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell;
- a number of wordlines (30-33) coupled to the gate region of at least one memory cell;
- a strapping line (112) of lower resistance than the wordlines coupled to a single continuous wordline (31) in a single array (memory bank 100) wherein the strapping line bypasses only a portion in a middle region between a first and

second end of the single continuous wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch (figure 2B shows that distance between strapping lines 112 and 113 is greater than a wordline pitch between wordlines 31 and 32); and wherein the strapping line (112) bypasses only a portion a wordline within the single memory array (memory bank 100) and bypasses a different portion of a wordline within the single array than an adjacent strapping line (Figure 2A shows strapping line 112 bypasses a different portion of a wordline than strapping lines 110 or 111); and

- at least two channels (such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single wordline.

5. Regarding claim 2, Cowles also teaches that the strapping line comprises metal (column 4, first paragraph).

6. Regarding claim 3, Cowles also teaches the strapping line metal comprises a refractory metal (column 4, first paragraph).

7. Regarding claim 4, Cowles teaches that the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline (two middle memory arrays in figure 2A are considered as a first half of the memory cells).

8. Regarding claims 8-14, 15-18, 26-29, since the claims recite similar limitations as in claims 1-4, they are rejected on the same ground.

Claim Rejections - 35 USC § 102

9. Claims 5-7, 19-25, 30-36, 37-41, 45-48, and 49-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

10. Regarding claim 5, Cowles discloses a memory array (figures 2A, 2B) comprising:

- a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region;
- a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell;
- a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell;
- a number of wordlines (30-33 in figure 2A) coupled to the gate region of at least one memory cell;
- a plurality of separate strapping lines (110-113) of lower resistance than the wordlines coupled to at least one of the number of wordlines (wordline 31) in a single array (memory block 100) wherein the strapping lines bypass a plurality of separate portions of a single continuous wordline (column 3, lines 57-60), and wherein adjacent strapping lines (110, 112) bypass only a portion of a wordline within the memory array and bypass different portions of adjacent wordlines within the memory array (Figure 2A shows strapping line 112 bypasses a different portion of a wordline than strapping lines 110 or 111); and

- a plurality of channels (such as node 150 in figure 2A) connecting the plurality of strapping layers to the wordline.

11. Regarding claim 6, Cowles also teaches that the strapping line comprises metal (column 4, first paragraph).

12. Regarding claim 7, Cowles also teaches the strapping line metal comprises a refractory metal (column 4, first paragraph).

13. Regarding claims 19-25, 30-36, 37-41, 45-48 and 49-54, since the claims recite similar limitations as in claims 5-7, they are rejected on the same ground.

Claim Rejections - 35 USC § 102

14. Claims 55-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Cowles (U.S. Patent 5,940,315).

Regarding claim 55, Cowles teaches a memory device (figures 2A,2B) comprising: a memory array (100) including a number of memory cells; an even row decoder (EVEN) located on a first side of the memory array; an odd row decoder (ODD) located on a second side of the memory array; a single column decoder (consisting of COL DEC 40 and 41) connected to the memory array; a number of parallel wordlines (30, 31, 32, 33) local to the memory array coupled to gate regions of memory cells, including one or more even wordlines (30, 32) coupled to the even row decoder, and one or more odd wordlines (31, 33) coupled to the odd row decoder, the odd wordlines arranged alternately with the even wordlines; and a number of strapping lines having lower resistance than the wordlines and connected to bypass portions of the wordlines

within the memory array (see column 4, lines 5-11), wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder.

Regarding claim 56, Cowles teaches that the even row decoder (EVEN) is located directly adjacent the first side and the odd row decoder (ODD) is located directly adjacent the second side.

Regarding claim 57, Cowles teaches a strapping line (110) connected to an odd wordline bypasses only one half of the wordline within the memory array nearer the odd row decoder and a strapping line (112) connected to an even wordline bypasses only one half of the wordline within the memory array nearer the even row decoder (In this rejection, the MEMORY ARRAYS 20 and 21 is considered as the memory array as claimed.)

Response to Arguments

15. Applicant's arguments filed 11-30-05 and 12-08-05 have been fully considered but they are not persuasive.

On page 14 of the Remarks the Applicant contends that “the Office Action admits that Cowles does not show “a number of memory cells," a number of source lines" or "a number of bit lines" (see Office Action pages 2 and 3). As such, the Office Action has not made a prima facie case of anticipation.” This contention is erroneous. Cowles does not show these elements in the drawings because they are inherent in Cowles’

teachings. Reading any reference cited in the References Cited of Cowles, one would find all these limitations. Memory cells must connect to source lines and bit lines in order to write/read data to/from the memory cells. By the principle of inherent, Cowles need not to show them.

The Applicant further argues that "the Office Action asserts that the memory bank 100 of Cowles reads on the single memory array recited in claim 1 (see Office Action pg. 3). However, the memory bank 100 of Cowles is made of more than one memory array (see FIG. 2A), and Cowles states that the invention . .. may be used with any number of arrays greater than one (see col. 3 lines 23-27). Thus, Cowles does not disclose the structure recited in claim 1." This statement is also not correct. Cowles ponders any number of arrays to be applied to the invention with purpose of reducing a word line's resistance by using metal strapping lines. So the numbers of arrays as taught by Cowles is variable in according to needs. For example, in figure 2A of Cowles, the array may include only two MEMORY ARRAYS (20, 21).

In summary, all the claims in the instant application are unpatentable.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

01-25-06

Son L. Mai
Primary Examiner
Art Unit 2827